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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,099	03/01/2004	Eric Chen-Li Sheng	TRAN-P283	2474

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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/791,099	SHENG ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-33* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-10, 12-14, 26-29 and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Ando (U.S. Pub. No. 20040111231).

With respect to claims 1, 8 and 27, Ando teaches a computer-implemented method and computer software program that implements the method of reducing temperature variation among integrated circuits during burn-in testing, comprising: measuring power consumed by an integrated circuit under test (section 0030); measuring an ambient temperature associated with said integrated circuit under test (section 0035); and adjusting a body bias voltage of said integrated circuit under test to achieve a desired junction temperature of said integrated circuit under test (section 0035).

With respect to claims 2, 3, 5-7, 9, 10, 12-14, 26, 28, 29 and 31-33, Ando further teaches: said ambient temperature is measured for a region comprising only said integrated circuit under test (sections 0019 and 0035); said ambient temperature is

measured for a region comprising more than one integrated circuits under test (sections 0019 and 0035); an operating voltage of said integrated circuit under test remains fixed during said measuring and said adjusting (section 0033); said body bias voltage is individually controllable for said integrated circuit under test (section 0035); said integrated circuit under test comprises body-biasing well structures to accept said body bias voltage (section 0020); and said method implemented by said test controller also comprises stimulating said integrated circuit for testing (section 0025).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 11, 19-25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Chandrakasan et al. (U.S. Pub. No. 20040183588).

With respect to claim 19, Ando teaches a system for testing an integrated circuit comprising: an operating voltage supply for coupling said integrated circuit (sections 0019 and 0020); a body bias voltage supply for coupling said integrated circuit for providing a body bias voltage (sections 0019 and 0020); an ambient temperature sensor for determining an ambient temperature for a region proximate to said integrated circuit (section 0035); a test controller for coupling said integrated circuit, said bias voltage

supply and said ambient temperature sensor, said test controller for implementing a method for reducing temperature variation among an integrated circuit during burn-in testing (sections 0019, 0020, 0035), said method comprising: accessing a measure of power consumed by said integrated circuit (sections 0075 and 0079); accessing a measure of ambient temperature associated with said integrated circuit (section 0035); and adjusting said body bias voltage of said integrated circuit to achieve a desired junction temperature of said integrated circuit (section 0035).

Ando does not mention expressly a current measuring device for coupling said integrated circuit for measuring operating current of said integrated circuit.

Chandrakasan et al. disclose a method for optimizing power utilization by digital integrated circuit, and teach a current measuring device for coupling said integrated circuit for measuring operating current of said integrated circuit (section 0113).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Chandrakasan et al. in the invention of Ando in order to measure power consumption accurately and directly from measurements of current to said integrated circuit because power is current times voltage (Ando, section 0022; Chandrakasan et al., section 0113).

With respect to claims 20, 21 and 23-25, Ando further teaches: said ambient temperature is measured for a region comprising only said integrated circuit under test (sections 0019 and 0035); said ambient temperature is measured for a region comprising more than one integrated circuits under test (sections 0019 and 0035); an operating voltage of said integrated circuit under test remains fixed during said

measuring and said adjusting (section 0033); said body bias voltage is individually controllable for said integrated circuit under test (section 0035); said integrated circuit under test comprises body-biasing well structures to accept said body bias voltage (section 0020).

With respect to claims 4, 11, 22 and 30, Ando teaches the method and system that includes the subject matter discussed above except that said measuring power comprises measuring current to said integrated circuit under test.

Chandrakasan et al. disclose a method for optimizing power utilization by digital integrated circuit, and teach the step of measuring power that comprises measuring current to said integrated circuit under test (section 0113).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Chandrakasan et al. in the invention of Ando in order to measure power consumption accurately and directly from measurements of current to said integrated circuit because power is current times voltage (Ando, section 0022; Chandrakasan et al., section 0113).

5. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Cohen et al. (US Provisional Application 60/500,561).

Ando teaches a computer implemented method of determining a junction temperature of an integrated circuit, said method comprising: measuring an ambient temperature in a region proximate to said integrated circuit (section 0035); measuring electrical power utilized by said integrated circuit (section 0030); and determining a junction temperature of said integrated circuit (section 0035).

Ando does not mention expressly: accessing a thermal resistance value for said integrated circuit; and said thermal resistance value is accessed from a computer usable media.

Cohen et al. disclose methods and apparatus for controlling the performance of integrated circuits having a thermal limitation, and teach: using a thermal resistance value of said integrated circuit for controlling the performance of said integrated circuit, and said thermal resistance value is accessed from a computer usable media (Figs. 1 and 2; the "Description" and "Appendix" sections).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Cohen et al. in the invention of Ando in order to consider the impacts of external factors such as the ambient temperature, and inherent features of the microprocessor technology, such as the thermal resistance to heat flow from the IC junction to the ambient air, on the performance of said integrated circuit (Ando, section 0003; Cohen et al., the "Background" section).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Cohen et al., as applied to claim 15 above, and further in view of Chandrakasan et al.

Ando in view of Cohen et al. teach the method that includes the subject matter discussed above except that said measuring electrical power comprises measuring current to said integrated circuit.

Chandrakasan et al. teach measuring electrical power by measuring current to said integrated circuit (Section 113).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Chandrakasan et al. in the combination of Ando and Cohen et al. in order to measure power consumption accurately and directly from measurements of current to said integrated circuit because power is current times voltage (Ando, section 0022; Chandrakasan et al., section 0113).

Allowable Subject Matter

7. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

8. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claim 16 is the inclusion of the claimed method step of multiplying said thermal resistance value by said electrical power and adding said ambient temperature. It is this limitation found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art Citations

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Butler (U.S. Pub. No. 2004018867) is entitled "System for and method of assessing chip acceptability and increasing yield".

2) Fan (U.S. Pub. No. 20040083075) is entitled "Junction temperatures measurements in semiconductor chip package technology".

Response to Arguments

10. Applicant's arguments received 09/16/05 with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1-33 are rejected as new prior art reference (U.S. Pub. No. 20040111231 to Ando) has been found to teach the limitations: "measuring power consumed by an integrated circuit under test", "measuring an ambient temperature associated with said integrated circuit under test", "adjusting a body bias voltage of said integrated circuit under test to achieve a desired junction temperature of said integrated circuit", and other limitations discussed in sections 2, 4 and 5 set forth above in this office action.

Applicant argued that Chandrakasan et al. do not teach "measuring current to said integrated circuit under test". The Examiner's position is that the Chandrakasan patent does teach this limitation (see section 4 above for details).

Regarding the Cohen reference, citations to the corresponding US Provisional Application 60/500,561, to which the Cohen reference claims benefit, are made in supporting the rejections, as set forth above in this office action.

Regarding claims 15, 17 and 18, Applicant's arguments against the references individually is noted. Applicant is reminded that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, it is deemed that the combined teachings of the cited prior art references would have suggested to those of ordinary skill in the art a method of determining a junction temperature of an integrated circuit including all the limitations recited in these claims, as delineated in sections 5 and 6 set forth above in this office action.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

XS
November 21, 2005

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